SCSI Active Terminator

FEATURES

- Complies with SCSI, SCSI-2 Standards
- 10pF Channel Capacitance During Disconnect
- Active Termination for 18 Lines
- Logic Command Disconnects all Termination Lines
- Low Supply Current in Disconnect Mode
- Trimmed Regulator for Accurate Termination Current
- Current Limit and Thermal Shutdown Protection
- 110 Ohm Termination
- Meets SCSI Hot Plugging

DESCRIPTION

The UC5601 provides precision resistive pull-up to a 2.9V reference for all 18 lines in a Small Computer Systems Interface (SCSI) bus cable. The SCSI-2 standard recommends active termination at both ends of every cable segment utilizing single ended drivers and receivers.

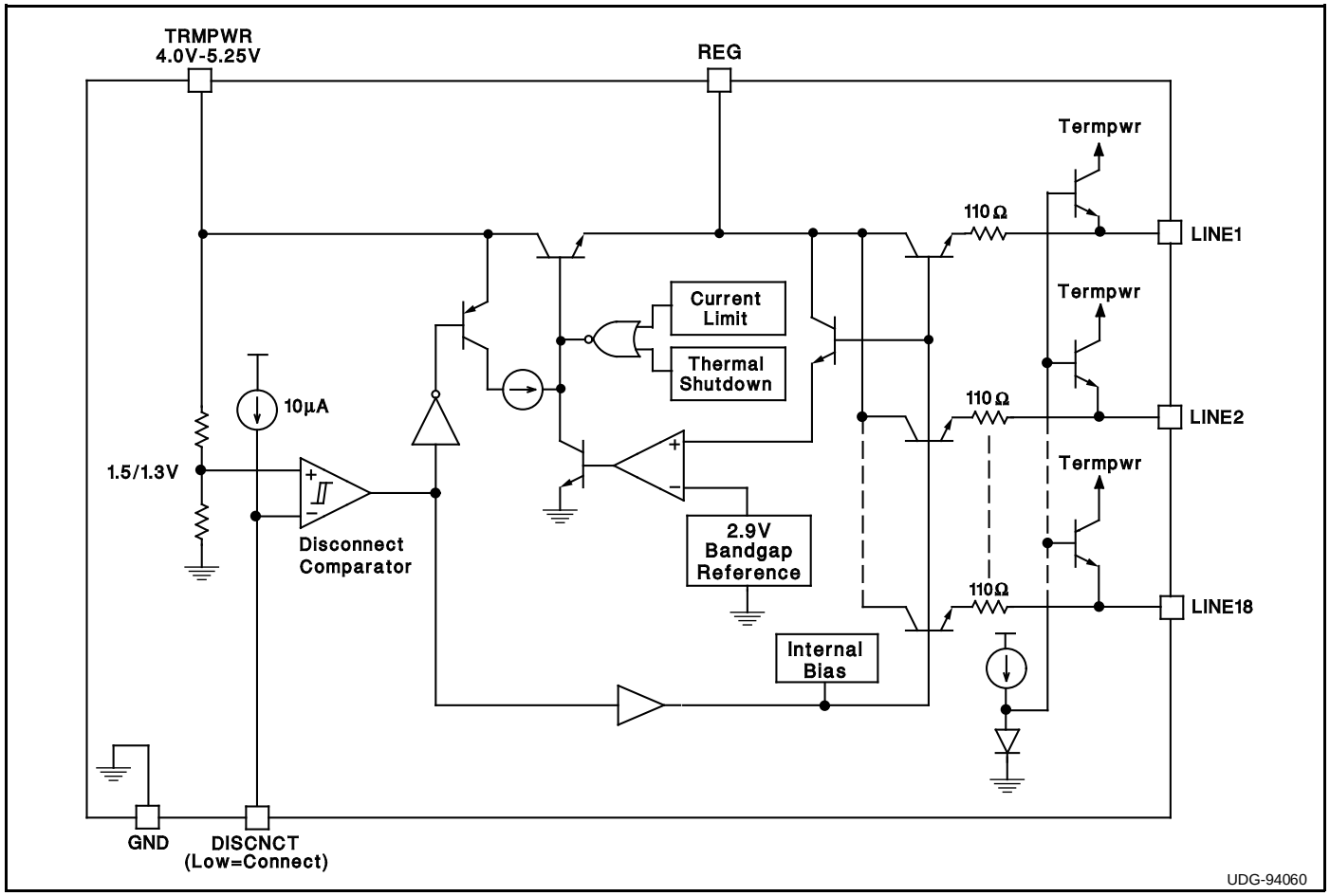
Internal circuit trimming is utilized, first to reduce resistor tolerances to ±3% and then to adjust the regulator's output voltage to insure termination current accuracy of ±3%.

The UC5601 provides a disconnect feature which, upon a logic command, disconnects all terminating resistors, and turns off the regulator; greatly reducing standby power.

Other features include negative clamping on all signal lines, 20mA of active negation sink current capability, regulator current limiting, and thermal shutdown protection.

This device is offered in low thermal resistance versions of the industry standard 28 pin wide body SOIC and PLCC, as well as a 24 pin DIL plastic package.

BLOCK DIAGRAM



Circuit Design Patented

ABSOLUTE MAXIMUM RATINGS

Termpwr Voltage . . . . . +7V
Signal Line Voltage . . . . . 0V to +7V
Regulator Output Current 1A
Storage Temperature . . . . . –65°C to +150°C
Operating Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) . . . . . +300°C

Unless otherwise specified all voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal.

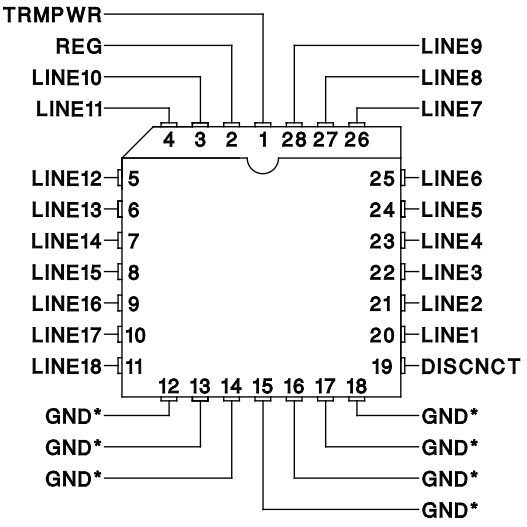
Consult Packaging Section of Unitrode Integrated Circuits databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

Termpwr Voltage . . . . . 4.0V to 5.25V
Signal Line Voltage . . . . . 0V to +3V
Disconnect Input Voltage . . . . . 0V to Termpwr

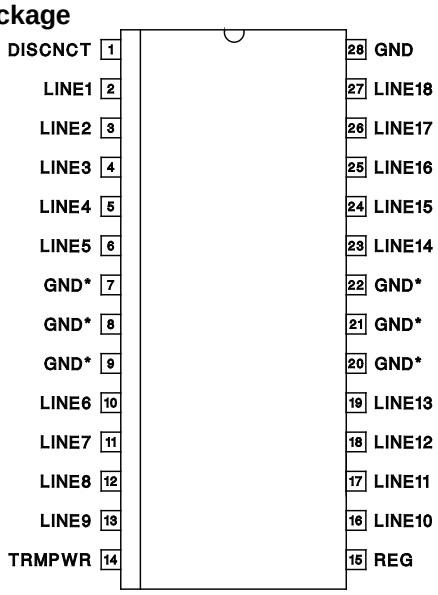
CONNECTION DIAGRAMS

PLCC-28 (Top View)
QP Package



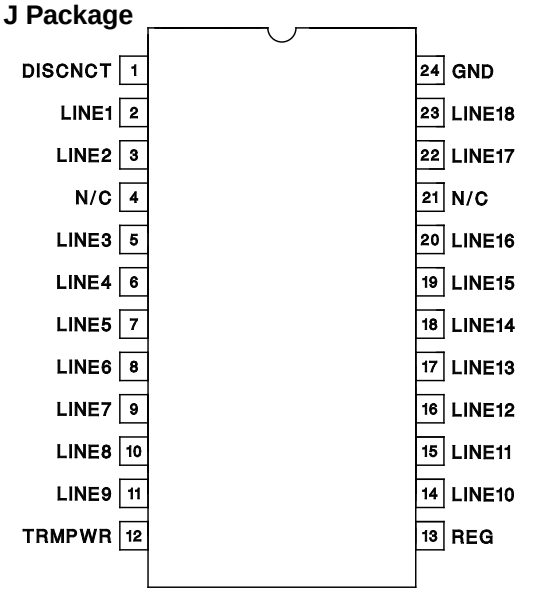
** QP package pins 12 - 18 serve as both heatsink and signal ground.*

SOIC-28 (Top View)
DWP Package



** DWP package pin 28 serves as signal ground; pins 7, 8, 9, 20, 21, 22 serve as heatsink/ground.*

DIL-24 (Top View)
N or J Package



Note: Drawings are not to scale.

ELECTRICAL CHARACTERISTICS Unless otherwise stated, these specifications apply for T_A = 0°C to 70°C. TRMPWR = 4.75V, DISCNCT = 0V. T_A = T_J.

PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNITS
Supply Current Section							
Termpwr Supply Current	All termination lines = Open				17	25	mA
	All termination lines = 0.5V				400	430	mA
Power Down Mode	DISCNCT = Open				100	150	µA
Output Section (Termination Lines)							
Termination Impedance	ΔI_{LINE} = -5mA to -15mA			107	110	113	Ω
Output High Voltage	V_{TRMPWR} = 4V (Note 1)			2.65	2.9		V
Max Output Current	V_{LINE} = 0.5V			-21.1	-21.7	-22.4	mA
	V_{LINE} = 0.5V, TRMPWR = 4V (Note 1)			-19.8	-21.7	-22.4	mA
Output Clamp Level	I_{LINE} = -30mA			-0.2	-0.05	0.1	V
Output Leakage	DISCNCT = 4V	TRMPWR = 0V to 5.25V REG = 0V	V_{LINE} = 0 to 4V		10	400	nA
			V_{LINE} = 5.25V			100	µA
		TRMPWR = 0V to 5.25V, REG = Open V_{LINE} = 0V to 5.25V			10	400	nA
Output Capacitance	DISCNCT = Open (Note 2)				10	12	pF
Regulator Section							
Regulator Output Voltage				2.8	2.9	3.0	V
Line Regulation	TRMPWR = 4V to 6V				10	20	mV
Load Regulation	I_{REG} = 0 to -400mA				20	50	mV
Drop Out Voltage	All Termination Lines = 0.5V				1.0	1.2	V
Short Circuit Current	V_{REG} = 0V			-450	-650	-850	mA
Current Sink Capability	V_{REG} = 3.5V			8	20	25	mA
Thermal Shutdown					170		°C
Disconnect Section							
Disconnect Threshold				1.3	1.5	1.7	V
Threshold Hysteresis				100	160	250	mV
Input Current	DISCNCT = 0V				10	15	µA

Note 1: Measuring each termination line while other 17 are low (0.5V).
Note 2: Guaranteed by design. Not 100% tested in production.

THERMAL DATA

QP package: (see packaging section of UICC data book for more details on thermal performance)

Thermal Resistance Junction to Leads, θjL . . . . . 15°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 30°-40°C/W

DWP package:

Thermal Resistance Junction to Leads, θjL . . . . . 18°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 33°-43°C/W

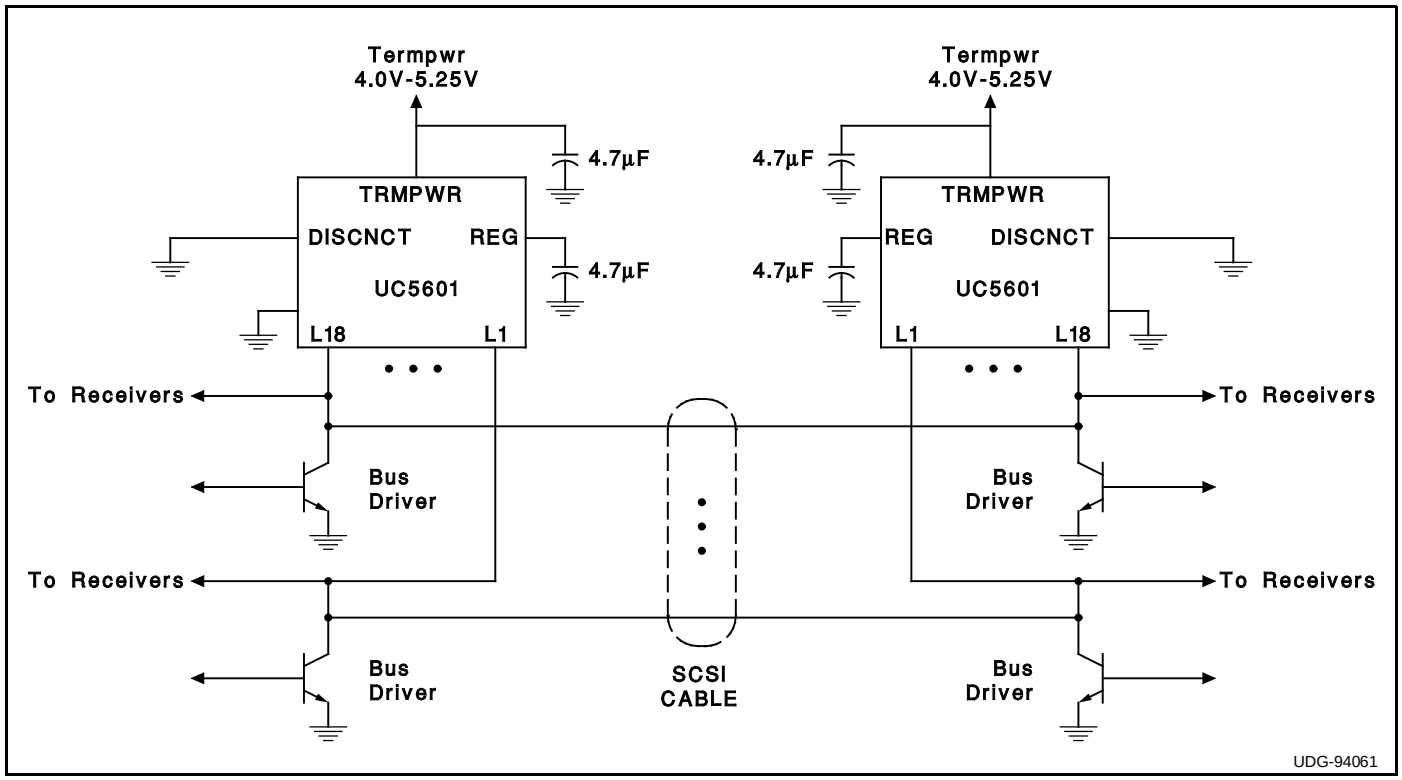
J package:

Thermal Resistance Junction to Leads, θjL . . . . . 40°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 75°-85°C/W

N package:

Thermal Resistance Junction to Leads, θjL . . . . . 50°C/W
Thermal Resistance Junction to Ambient, θja . . . . . 95°-105°C/W

Note: The above numbers for θjL are maximums for the limiting thermal resistance of the package in a standard mounting configuration. The θja numbers are meant to be guidelines for the thermal performance of the device/pc-board system. All of the above numbers assume no ambient airflow.



Typical SCSI Bus Configuration Using the UC5601

A Look at the Response of a SCSI-2 Cable

Figure 1 shows a single line of a SCSI cable. The driver is an open colletor type which when asserted pulls low, and when negated the termination resistance serves as the pull-up.

Figure 2 shows a worst case scenario of mid cable de-assertion with a close proximity receiver. The voltage V_{STEP} is defined as:

$$V_{STEP} = V_{OL} + I_O Z_0$$

V_{OL} = Driver Output Low Voltage
I_O = Current from Receiving Terminator
Z_0 = Cable Characteristic Impedance

$$I_O = \frac{V_{REG} - V_{OL}}{110}$$

In the pursuit of higher data rates, sampling culd occur during this step portion, therefore it is important to ensure that the step is as high as possible to get the most noise margin. For this reason the UC5601 is trimmed so that the output current (I_O) is as close as possible to the SCSI max current spec of 22.4mA. The Termination impedance is initially trimmed on the IC to 110 ohms typical, then the regulator voltage is trimmed for the highest output current to within 22.4mA.

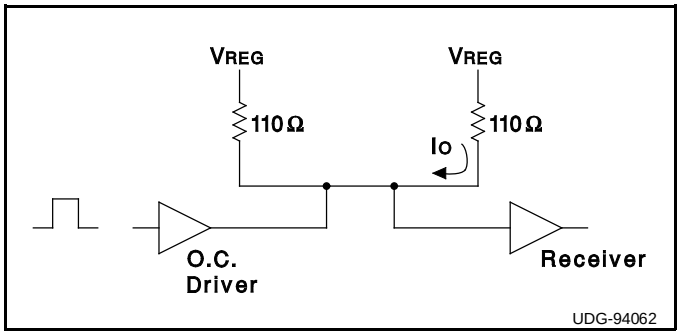


Figure 1. A Single Line of a SCSI Cable

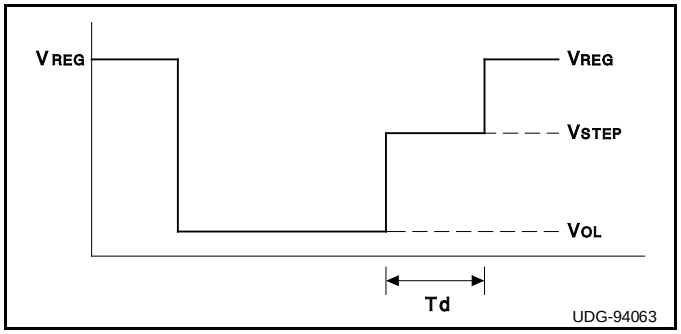


Figure 2. A Typical Response of a SCSI Cable

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC5601DWP	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-2-260C-1 YEAR
UC5601DWPG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-2-260C-1 YEAR
UC5601DWPTR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-2-260C-1 YEAR
UC5601DWPTRG4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	Cu NiPdAu	Level-2-260C-1 YEAR
UC5601N	ACTIVE	PDIP	N	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC5601NG4	ACTIVE	PDIP	N	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC5601QP	ACTIVE	PLCC	FN	28	37	TBD	Cu NiPdAu	Level-2-220C-1 YEAR
UC5601QPTR	ACTIVE	PLCC	FN	28	750	TBD	Cu NiPdAu	Level-2-220C-1 YEAR

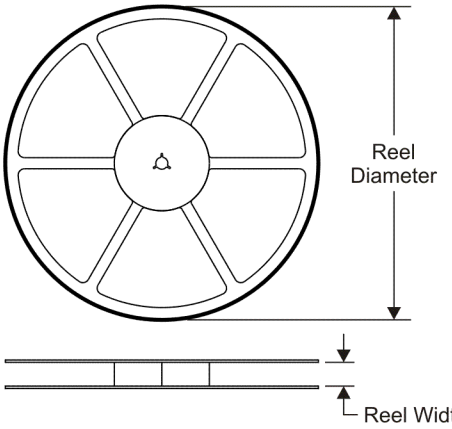
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

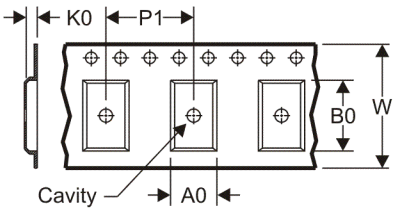
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

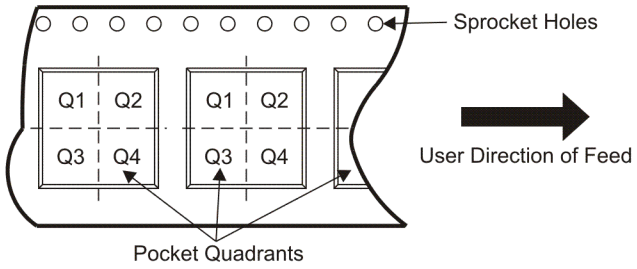


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

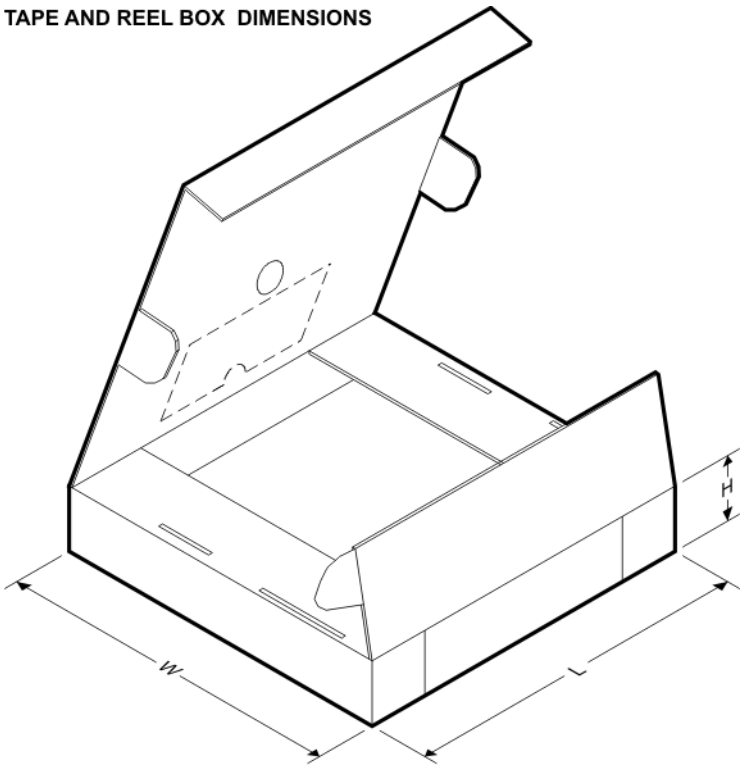
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC5601DWPTR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
UC5601QPTR	PLCC	FN	28	750	330.0	24.4	12.95	12.95	5.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

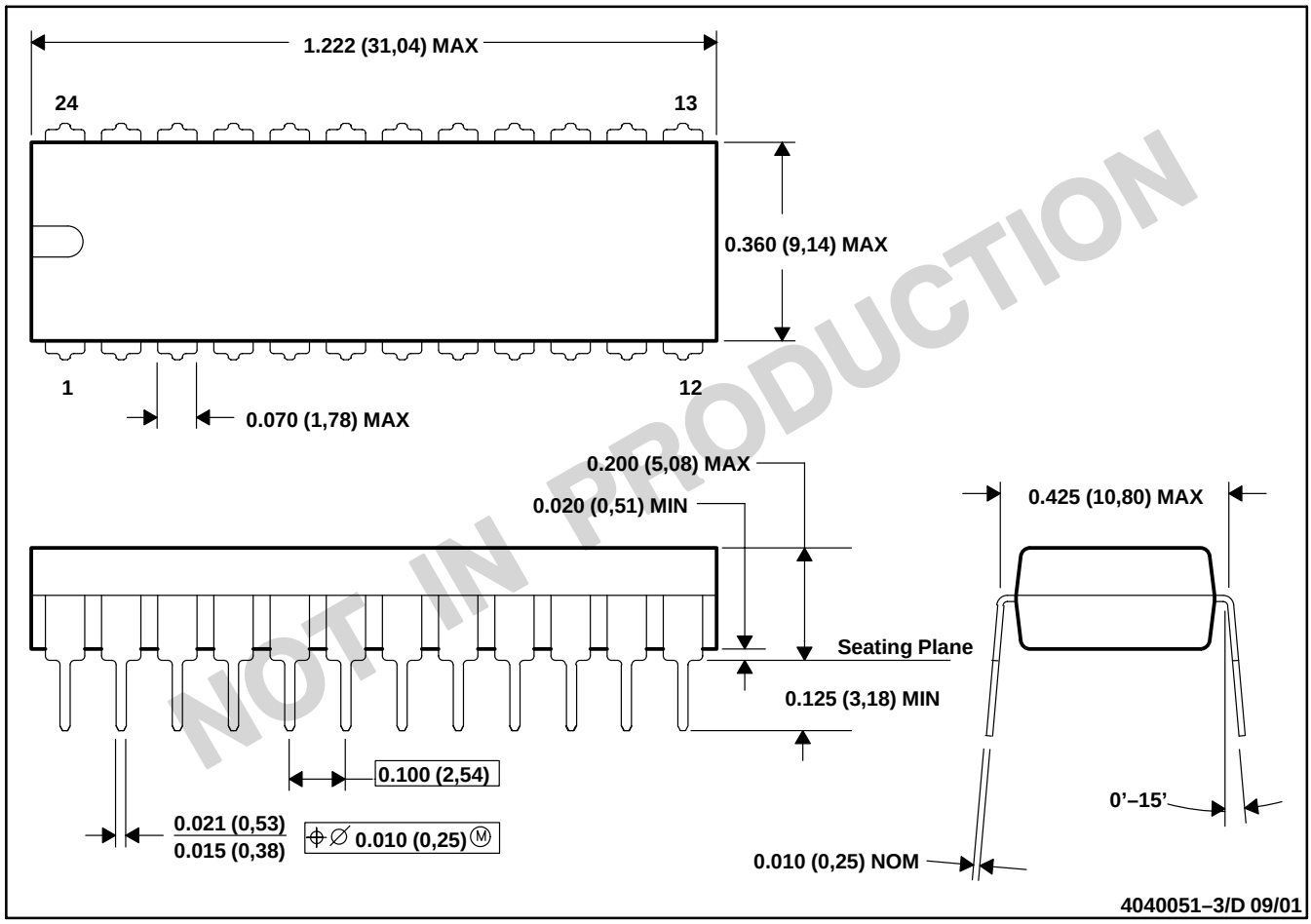


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC5601DWPTR	SOIC	DW	28	1000	346.0	346.0	49.0
UC5601QPTR	PLCC	FN	28	750	346.0	346.0	41.0

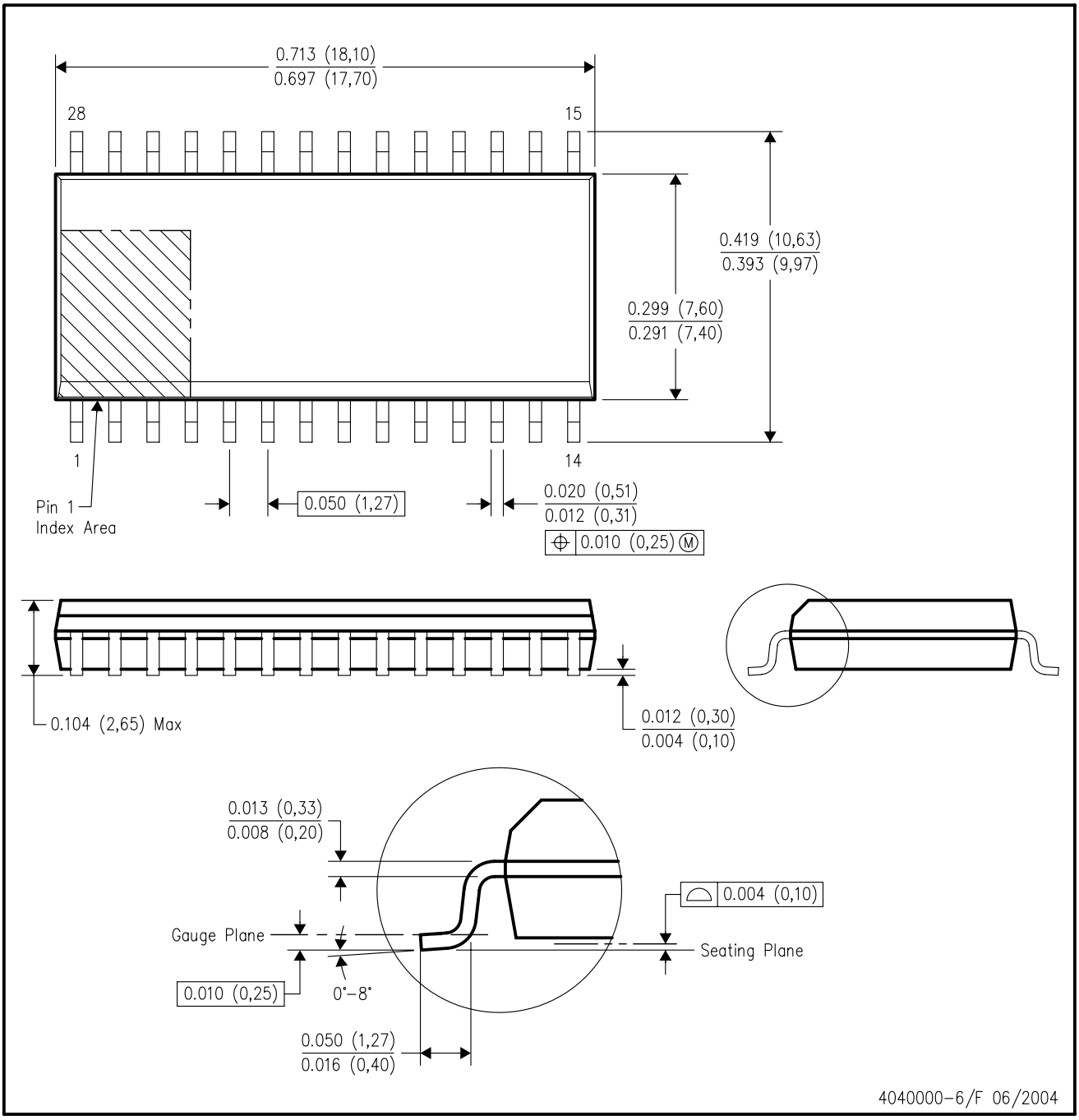
MPDI006B – SEPTEMBER 2001 – REVISED APRIL 2002

N (R–PDIP–T24) **PLASTIC DUAL–IN–LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–010

DW (R–PDSO–G28) PLASTIC SMALL–OUTLINE PACKAGE



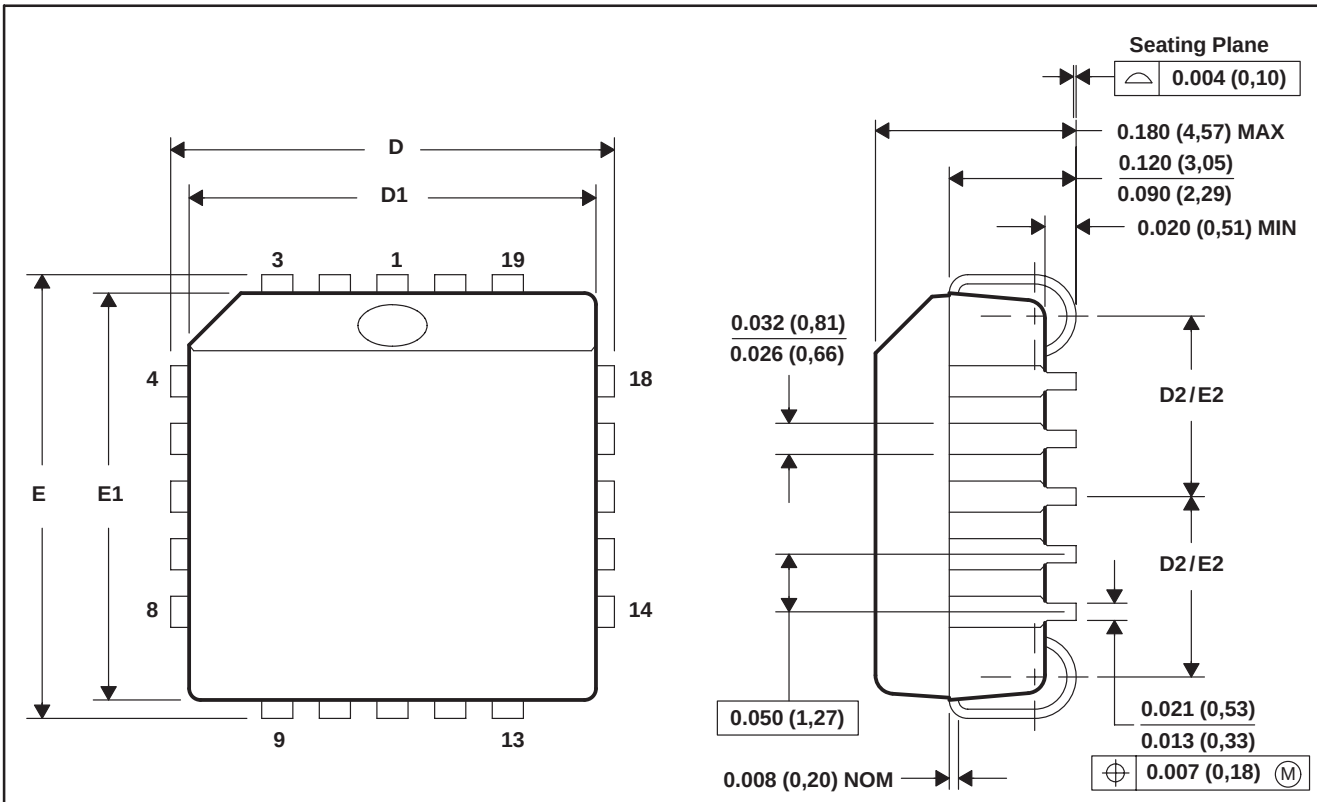
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

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NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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